NOTICE OF I	Form Approved OMB No. 0704-0188						
Public reporting burden for this collection reviewing instructions, searching existing completing and reviewing the collection of other aspect of this collection of informat Defense, Washingtion Headquarters Services, Davis Highway, Suite 1204, Arlington, VA 22 Reduction Project (0704-0188), Washington, ADDRESSED. RETURN COMPLETED FORM TO THE GO	eded, and	2. PROCURING ACTIVITY NO.					
ACTIVITY NUMBER LISTED IN ITEM 2 OF THIS FO	3. DODAAC						
4. ORIGINATOR	b. ADDRESS (Street, City, St Defense Electronics	Supply Center	5. CAGE CODE 67268	6. NOR NO. 5962-R049-94			
a. TYPED NAME (First, Middle Initial, Last)	1507 Wilmington Pike Dayton, OH 45444-527		7. CAGE CODE 67268	8. document no. 85152			
9. TITLE OF DOCUMENT		10. REVISIO	N LETTER	11. ECP NO.			
MICROCIRCUITS, MEMORY, DIGITAL, MONOLITHIC SILICON	NMOS, 256K x 1 RAM	a. CURRENT D	b. NEW E				
12. CONFIGURATION ITEM (OR SYSTE	EM) TO WHICH ECP APPLIES	3					
All							
13. DESCRIPTION OF REVISION							
Sheet 1: Revisions ltr column; add "E".  Revisions description column; add "Changes in accordance with NOR 5962-R049-94".  Revisions date column; add "93-12-01".  Revision level block; add "E".  Rev status of sheets; For sheets 15 and 28 add "E".							
.020 inch (0.51 mm) k	Sheet 15: Footnote number 19: Change from Must be a dimensional difference of .020 inch (0.51 mm) between L1 and L2. To read as follows:  Must be a dimensional difference of .010 inch (0.25 mm)between L1 and L2.						
Revision level Block	s; add "E"						
Sheet 28: Figure 6: Change fro the ± 20%	om " $C_L = pF \pm 20$ %" To $C_L$	= 80 pF and del	Lete				
Revision level Block	c; add "E"						
14. THIS SECTION FOR GOVERNMENT USE ONLY							
a. (X one) X (1) Existing document supplemented by the NOR may be used in manufacture.							
(2) Revised document must be received before manufacturer may incorporate this change.							
(3) Custodian of master document shall make above revision and furnish revised document.							
b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT c. TYPED NAME (First, Middle Initial, Last)  DESC-EC Michael A. Frye							
d. TITLE	e. SIGNATURE		f. DATE SIGNED				
Chief, Microelectronics Branch	Michael A. Frye		(YYMMDD) 93-12-01				
15a. ACTIVITY ACCOMPLISHING REVISION b. REVISION COMPLETED (Signature) c. DATE SIGNED (YYMMDD)							

93-12-01

LTR	DESCRIPTION	DATE (YR-MO- DA)	APPROVEI		
A	Convert to military drawing format. Add LCC package type. Add one device type. Change replacement military specification number. Add two vendors.	87-05-05	M. A. Frye		
В	Add vendor CAGE number 6Y440 as a supplier of device type 03. Changes to table I and table I footnotes. Changes to figure 1, figure 3, and figure 5. Editorial changes throughout.	88-10-04	M. A. Frye		
С	Delete vendor CAGE 01295 as a source of supply for X package. Add the Y package for vendor CAGE 01295. Editorial changes throughout.	90-11-06	M. A. Frye		
D	Changes to figure 1, case outline Y, dimensions for symbols L1 and L2. Editorial changes throughout.	92-07-27	M. A. Frye		

# CURRENT CAGE CODE 67268

REV																					
SHEET																					
REV	D	U	C	С	С	U	C	U	C	C	U	С	С	С	C	D					
SHEET	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					
REV STATUS				REV	7		D	D	D	С	В	В	В	В	С	С	С	C	С		
OF SHEETS				SHE	ET		1	2	3	4	5	6	7	8	9	10	11	12	13		
PMIC N/A				PREPARED BY James E. Jamison  DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444							€R										
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					D					SI	HEET	:	1		OF		29				

## 1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 <u>Device type(s)</u>. The device type(s) shall identify the circuit function as follows:

Device type	Generic number	<u>1</u> /	<u>Circuit</u>	Access time	Refresh
01			256K x 1 DRAM	150 ns	256 cycles (4 ms)
02			256K x 1 DRAM	200 ns	256 cycles (4 ms)
03			256K x 1 DRAM	120 ns	256 cycles (4 ms)

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

#### Outline letter Case outline

E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
X	See figure 1 (18-terminal, .305" x .505"), rectangular chip carrier package
Y	See figure 1 (18-terminal, .305" x .505"), rectangular chip carrier package

1.3 Absolute maximum ratings. 2/

Voltage range for any pin, including $V_{CC}$ supply $\frac{3}{2}$	-1.0 V dc to +7.0 V dc
Short circuit output current	50 mA
Power dissipation	1 W
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case $(\Theta_{,TC})$ :	
Cases X and Y	50°C/W
Case E	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage range ( $V_{CC}$ )	4.75 V dc to 5.25 V dc
Supply voltage (V <sub>SS</sub> )	0 V dc
High level input voltage range (V <sub>IH</sub> )	2.4 V dc to 5.0 V dc
Low level input voltage range (V <sub>IL</sub> )	-0.5 V dc to +0.6 V dc
Case operating temperature range (T <sub>C</sub> )	-55°C to +110°C
Refresh cycle time	4.0 ms

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET 2

Generic numbers are listed on the Standarized Military Source Approval Bulletin and will be listed in MIL-BUL-103.

Voltage values are with respect to  ${
m V}_{
m SS}$ . Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

#### 2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standard, and bulletin</u>. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

- 2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.
  - 3. REQUIREMENTS
- 3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.
  - 3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.
  - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.
  - 3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.
  - 3.2.4 Block diagram. The block diagram shall be as specified on figure 4.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.
- 3.5 <u>Marking</u>. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE <b>A</b>		85152
	REVISION LEVEL D	SHEET 3

Test	Symbol	Conditions 1/2/	Group A	Device	Limi	Unit	
		$-55^{\circ}C \le T_{C} \le +110^{\circ}C$ 4.75 V dc $\le V_{CC} \le 5.25$ V dc	subgroups	type	Min	Max	T
High level output voltage	v <sub>OH</sub>	$I_{OH} = -5 \text{ mA}, V_{CC} = 4.75 \text{ V}$ $V_{IL} = 0.6 \text{ V}, V_{IH} = 2.4 \text{ V}$	1,2,3	All	2.4		v
Low level output voltage	v <sub>ol</sub>	$I_{OL}$ = 4.2 mA, $V_{CC}$ = 4.75 V	1,2,3	All		0.4	v
High level input leakage current	IIH	$v_{CC} = 5.25 \text{ V}, V_{I} = 5.0 \text{ V}$	1,2,3	All		10	μА
Low level input leakage current	I <sub>IL</sub>	$v_{CC} = 5.25 \text{ V}, V_{I} = 0.0 \text{ V}$	1,2,3	All		-10	μΑ
High level output leakage current	I <sub>OH</sub>	V <sub>CC</sub> = 5.25 V V <sub>O</sub> = 5.25 V	1,2,3	All		10	μА
Low level output leakage current	I <sub>OL</sub>	$v_{CC} = 5.25 \text{ v}, v_{O} = 0.0 \text{ v}$	1,2,3	All		-10	μА
Average operating	I <sub>CC1</sub>	t <sub>c</sub> = minimum cycle	1,2,3	01		75	mA
current during read or write cycle $\frac{3}{2}$		V <sub>CC</sub> = 5.25 V		02		60	mA
				03		80	mA
Standby current $3/$	I <sub>CC2</sub>	After 1 memory cycle $\overline{RAS}$ and $\overline{CAS}$ high $V_{CC}$ = 5.25 V	1,2,3	All		5	mA
Average refresh	I <sub>CC3</sub>	t <sub>c</sub> = m <u>ini</u> mum cycle, CAS	1,2,3	01		60	mA
current <u>3</u> /		high, $\overline{RAS}$ cycling $V_{CC} = 5.25 \text{ V}$		02		50	mA
				03		63	mA
Average page-mode current 3/	I <sub>CC4</sub>	t <sub>c(P)</sub> = minimum cycle, RAS low, CAS cycling	1,2,3	01,03		50	mA
<u> </u>		V <sub>CC</sub> = 5.25 V		02		45	mA
Access time from RAS	t <sub>a(R)</sub>	See figures 5 and 6	9,10,11	01		150	ns
	a(x)	$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$		02		200	ns
				03		120	ns

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET 4

Test Symbol	Symbol	Conditions 1/2/	Group A	Device	Limi	its	Unit
		$-55^{\circ}C \le T_{C} \le +110^{\circ}C$ 4.75 V dc $\le V_{CC} \le 5.5$ V dc	subgroups	type	Min	Max	
Access time from CAS	t <sub>a(C)</sub>	See figures 5 and 6	9,10,11	01		80	ns
		$V_{CC} = 4.75 \text{ V to 5.25 V}$		02		100	ns
		 		03		65	ns
Ou <u>tpu</u> t disable time after	t <sub>dis(CH)</sub>		9,10,11	01		30	ns
CAS high $\frac{4}{}$ /				02		35	ns
				03		30	ns
Page-mode cycle time $\frac{4}{}$ /	t <sub>c(P)</sub>		9,10,11	01	145		ns
				02	190		ns
				03	125		ns
Page-mode cycle time (read-modify-write cycle 4/	t <sub>c(PM)</sub>		9,10,11	01	205		ns
				02	250		ns
				03	172		ns
Read cycle time $\frac{4}{}$	tc(rd)		9,10,11	01	260		ns
				02	330		ns
				03	230		ns
Write cycle time $\frac{4}{2}$	t <sub>c(W)</sub>		9,10,11	01	260		ns
				02	330		ns
				03	230		ns
Read-write/read-modify-	t <sub>c(rdW)</sub>		9,10,11	01	315		ns
write cycle time $\frac{4}{}$				02	390		ns
				03	277		ns
Pulse duration, CAS high	t <sub>w(CH)P</sub>		9,10,11	01	60		ns
(page mode)				02	80		ns
				03	50		ns

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET 5

TABLE I. <u>Electrical performance characteristics</u> - Continued.							
Test	Symbol	Conditions 1/2/	Group A	Device	Limits		Unit
		$-55^{\circ}C \le T_{C} \le +110^{\circ}C$ 4.75 V dc $\le V_{CC} \le 5.5$ V dc	subgroups	type	Min	Max	
Pulse duration, CAS high (non-page mode)	t <sub>w(CH)</sub>	See figures 5 and 6 V <sub>CC</sub> = 4.75 V to 5.25 V	9,10,11	01	60		ns
(non-page mode)		Vcc - 4:75 V 20 3:25 V		02	80		ns
		<u> </u>		03	25		ns
Pulse duration, CAS low	t <sub>w(CL)</sub>		9,10,11	01	80	10,000	ns
<u>5</u> /				02	100	10,000	ns
-		_		03	65	10,000	ns
Pulse duration, RAS high (precharge time) (page	t <sub>w(RH)P</sub>		9,10,11	01,02	120		ns
mode)			_	03	115		ns
Pulse duration, RAS high (precharge time)	t <sub>w(RH)</sub>		9,10,11	01,03	100		ns
(non-page mode)			-	02	120		ns
Pulse duration, RAS low	t <sub>w(RL)</sub>		9,10,11	01	150	10,000	ns
<u>5</u> /				02	200	10,000	ns
				03	120	10,000	ns
Write pulse duration	t <sub>w(W)</sub>		9,10,11	01	45		ns
				02	55		ns
				03	40		ns
Column address setup time	t <sub>su(CA)</sub>		9,10,11	All	0		ns
Row address setup time	t <sub>su(RA)</sub>		9,10,11	01,02	5		ns
-				03	0		ns
Data setup time	t <sub>su(D)</sub>		9,10,11	All	3		ns
Read command setup time	t <sub>su(rd)</sub>		9,10,11	All	5		ns
Early write command setup time before CAS low	t <sub>su(WCL)</sub>		9,10,11	All	0		ns

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET 6

Test Symbol	Symbol	Conditions 1/2/	Group A	Device	Limi	ts	Unit
		$-55^{\circ}\text{C} \leq \text{T}_{\text{C}} \leq +110^{\circ}\text{C}$ 4.75 V dc $\leq \text{V}_{\text{CC}} \leq 5.5$ V dc	subgroups	type	Min	Max	
Write command setup time	t <sub>su(WCH)</sub>	See figures 5 and 6	9,10,11	01	45		ns
before CAS high		$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$		02	65		ns
				03	40		ns
Write com <u>man</u> d setup time	t <sub>su(WRH)</sub>		9,10,11	01	45		ns
before RAS high				02	65		ns
				03	40		ns
Column a <u>ddr</u> ess hold time after CAS low	t <sub>h(CLCA)</sub>		9,10,11	01	30		ns
arter cab low				02	45		ns
				03	20		ns
Row address hold time th	t <sub>h(RA)</sub>		9,10,11	01	20		ns
				02	25		ns
				03	15		ns
Column a <u>ddr</u> ess hold time after RAS low	t <sub>h(RLCA)</sub>		9,10,11	01	100		ns
				02	145		ns
				03	75		ns
Data hold time after CAS	t <sub>h(CLD)</sub>		9,10,11	01	50		ns
10#				02	55		ns
				03	40		ns
Data hold time after RAS	t <sub>h(RLD)</sub>		9,10,11	01	120		ns
10W				02	155		ns
				03	95		ns
Data hold time after W	t <sub>h(WLD)</sub>		9,10,11	01	45		ns
low				02	55		ns
	}			03	40		ns

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET 7

		Electrical performance char					
Test	Symbol	Conditions $\underline{1}/\underline{2}/$ -55°C $\leq$ T <sub>C</sub> $\leq$ +110°C	Group A subgroups	Device type	Limits		Unit
		4.75 V dc < V <sub>CC</sub> < 5.5 V dc			Min	Max	
Read com <u>man</u> d hold time after CAS high	t <sub>h(CHrd)</sub>	See figures 5 and 6 V <sub>CC</sub> = 4.75 V to 5.25 V	9,10,11	All	0		ns
Read com <u>man</u> d hold time	t <sub>h(RHrd)</sub>		9,10,11	01,03	10		ns
after RAS high				02	15		ns
Write command hold time	t <sub>h(CLW)</sub>		9,10,11	01	50		ns
after CAS low				02	55		ns
				03	40		ns
Write command hold time	t <sub>h(RLW)</sub>		9,10,11	01	120		ns
				02	155		ns
				03	95		ns
Delay time, RAS low to CAS	t <sub>RLCH</sub>		9,10,11	01	150		ns
high				02	200		ns
				03	120		ns
De <u>lay</u> time, CAS high to RAS low	t <sub>CHRL</sub>		9,10,11	All	5		ns
Delay time, CAS low to RAS	t <sub>CLRH</sub>		9,10,11	01	80		ns
high				02	100		ns
				03	65		ns
Delay time, RAS low to CAS	t <sub>RLCH</sub>		9,10,11	01	30		ns
high <u>7</u> /				02	40		ns
				03	30		ns
Delay time, CAS low to RAS	t <sub>CLRL</sub>		9,10,11	01	30		ns
low <u>7</u> /				02	35		ns
				03	30		ns

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET 8

	TABLE I.	Electrical performance chara	cteristics -	Continued			
Test	Symbol	Conditions <u>1</u> / <u>2</u> /	Group A	Device type	Limits		Unit
		$-55^{\circ}C \le T_{C} \le +110^{\circ}C$ 4.75 V dc $\le V_{CC} \le 5.5$ V dc	subgroups		Min	Max	
Delay time, CAS low to W	t <sub>CLWL</sub>	See figures 5 and 6	9,10,11	01	85		ns
<pre>low (read-modify-write cycle only)</pre>		$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$		02	90		ns
				03	67		ns
De <u>lay</u> time, RAS high to CAS low	t <sub>RHCL</sub>		9,10,11	All	25		ns
Delay time, RAS low to	t <sub>RLCL</sub>		9,10,11	01	25	70	ns
CAS low				02	35	100	ns
				02	25	55	ns
Delay time, $\overline{RAS}$ low to $\overline{W}$	t <sub>RLWL</sub>		9,10,11	01	155		ns
<pre>low (read-modify-write cycle only)</pre>				02	190		ns
				03	122		ns
Refresh time interval	t <sub>rf</sub>		9,10,11	All		4.0	ms

- $\underline{1}$ / Timing measurements are referenced to  $V_{\mathrm{IL}}$  ma $\underline{\mathrm{xim}}$ um an $\underline{\mathrm{d}}$   $V_{\mathrm{IH}}$  minimum.
- System transition times (rise and fall) for RAS and CAS are to be a minimum of 3 ns and a maximum of
- $\underline{3}/$  All I<sub>CC</sub> measurements are taken with output (Q) open.
- $\underline{4}$ / All cycle times assume transition times  $t_t = 5$  ns.
- In a read-modify-write  $\underline{cyc}$ le  $t_{LWL}$  and  $t_{su(WCH)}$  must be observed. Depending on the user's transition time, this may require additional CAS low time  $t_{W(EL)}$ . Applies to page-mode read-modify-write also. In a read-modify-write cycle,  $t_{RLWL}$  and  $t_{su(WRH)}$  must be observed. Depending on the user's  $\underline{transition}$   $\underline{time}$ , this may require additional RAS low time  $t_{w(RL)}$ .
- 7/ CAS before RAS refresh only.
- 3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.
- Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.9 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET 9

- 4. QUALITY ASSURANCE PROVISIONS
- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
  - a. Burn-in test, method 1015 of MIL-STD-883.
    - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see  $3.6\ \mathrm{herein}$ ).
    - (2)  $T_A = +125^{\circ}C$ , minimum.
  - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. <u>Electrical test requirements</u>.

· .	
MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9, 10,
Group A test requirements (method 5005)	1, 2, 3, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8a, 8b

- \* PDA applies to subgroup 1.
- 4.3 <u>Quality conformance inspection</u>. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
  - 4.3.1 Group A inspection.
    - a. Tests shall be as specified in table II herein.
    - b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET 10

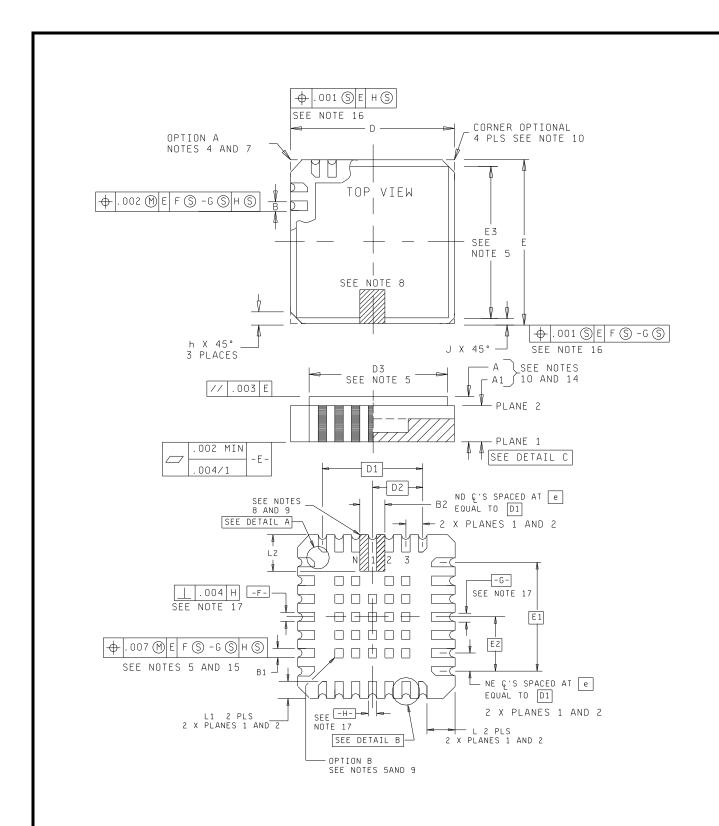


FIGURE 1. Case outlines X and Y (18-terminal, .305" x .505"), rectangular chip carrier package.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER		REVISION LEVEL	SHEET
DAYTON, OHIO 45444		D	11

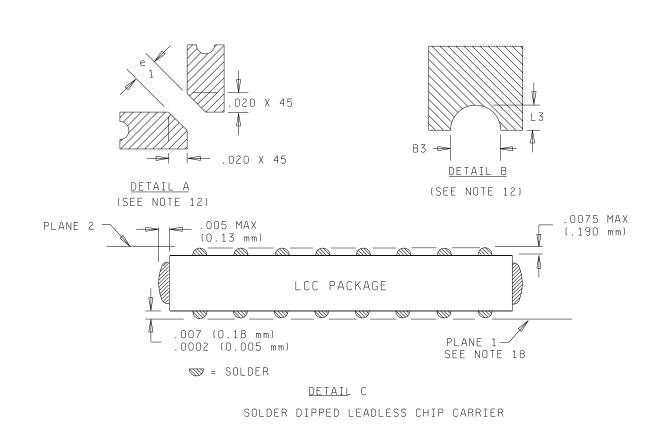


FIGURE 1. Case outlines X and Y (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET <b>12</b>

Dimensions					
	Inche	s	Millir	neters	
Symbol	Min	Max	Min	Max	Notes
A	.060	.120	1.52	3.04	10, 14
A1	.050	.088	1.27	2.24	
В					
B1	.022	.028	0.56	0.71	5, 7
В2	.072	REF	1.83	3 REF	8, 9
В3	.006	.022	0.15	0.56	12
D	.280	.305	7.11	7.74	
D1	.150	BSC	3.81	L BSC	
D2	.075	BSC	1.90	BSC	17
D3		.305		7.74	5
E	.480	.505	12.19	12.83	
E1	.200	BSC	5.08	B BSC	
E2	.100	BSC	2.54	4 BSC	17
E3		.365		9.27	5
e	.050	BSC	0.38	BSC	
e1	.015		5, 13	3	5, 13
h	.040	REF	1.02	2 REF	11
j	.020	REF	0.53	L REF	11
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	8, 9
L3	.003	.015	0.08	0.38	12
ND	4				6
NE	5				6
N	18				6

FIGURE 1. Case outline X (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER		REVISION LEVEL	SHEET
DAYTON, OHIO 45444		D	13

Dimensions					
	Inche	s	Millir	neters	
Symbol	Min	Max	Min	Max	Notes
A	.060	.120	1.52	3.04	10, 14
A1	.050	.088	1.27	2.24	
В					
B1	.020	.030	0.50	0.76	5, 7
В2	.072	REF	1.83	3 REF	8, 9
в3	.006	.022	0.15	0.56	12
D	.280	.305	7.11	7.74	
D1	.150	BSC	3.83	L BSC	
D2	.075	BSC	1.90	BSC	17
D3		.305		7.74	5
E	.480	.505	12.19	12.83	
E1	.200	BSC	5.08	BSC	
E2	.100	BSC	2.54	1 BSC	17
E3		.480		12.19	5
e	.050	BSC	0.38	BSC	
e1	.015		0.38		5, 13
h	.010	REF	0.25	5 REF	11
j	.010	REF	0.25	5 REF	11
L	.040	.055	1.14	1.40	
L1	.110	.120	2.79	3.05	19
L2	.120	.130	3.05	3.30	8, 9
L3	.003	.015	0.08	0.38	12
ND	4				6
NE	5				6
N	18				6

FIGURE 1. Case outline Y (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET <b>14</b>

#### NOTES:

- 1. Dimensions are in inches.
- 2. Metric equivalents are for general information only.
- 3. To specify options in detail specification, see figure C-7 of MIL-M-38510.
- 4. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals (see 50.6 of MIL-M-38510).
- 5. Unless otherwise specified, a minimum clearance of .015 inch (0.38 mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.).
- 6. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E" respectively.
- 7. The required plane 1 terminals and optional plane 2 terminals shall be electrically connected.
- 8. The index feature for terminal 1 identification, optical orientation or handling purposes, shall be within the shaded index areas shown on planes 1 and 2 (see 40.6.3 of MIL-M-38510). Plane 1 terminal 1 identification may be an extension of the length of the metallized terminal which shall not be wider than the B1 dimension. See note 9 for more details.
- 9. Plane 1 is the heat radiating surface. This surface may optionally be metallized with a checkerboard pattern of thermal conduction pads. The pad centerlines shall be aligned with the terminal centerlines. The number of pads in the pattern is determined by the following algorithm:

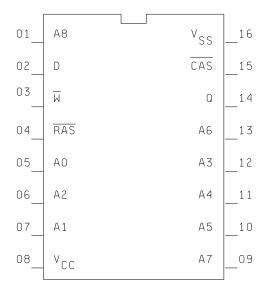
  (ND 2) x (NE 2) see note 6. When this option exists, the terminal 1 index feature may be additionally or alternately defined by deleting the thermal pad which is adjacent to terminal 1.
- 10. Dimension "A" controls the overall package thickness. When a window lid is used, dimension "A" must increase by a minimum of .010 inch (0.25 mm) and a maximum of .040 inch (1.02 mm).
- 11. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
- 12. See 50.6 and figure C-6 of MIL-M-38510. Dimensions "B3" minimum, "L3" minimum, and the appropriately derived castellation length define an unobstructed three dimensional space traversing all of the ceramic layers in which a castellation was designed. (Castellations are required on bottom two layers, optional on top ceramic layer.) Dimensions "B3" maximum and "L3" maximum define the maximum width and depth of the castellation at any point on its surface. Measurement of these dimensions may be made prior to solder dipping.
- 13. Corner metallization for terminals may have a .020 inch (0.51 mm) by  $45^{\circ}$  maximum chamfer to obtain the el dimension.
- 14. Chip carriers shall be constructed of a minimum of two ceramic layers.
- 15. The pad metallization, including annular ring, at the pad-to-package edge shall be within the virtual pad width established by true position dimensioning.
- 16. The tolerance is intended to limit package edge anomalies caused by material protrusions, such as rough ceramic, and misaligned ceramic layers.
- 17. When the number of terminals per side is even, datums F-G and -H- are located at the terminal array centers. When the number of terminals per side is odd, datums F-G and -H- are located at the centers of the center terminals.
- 18. See 40.2.3 of MIL-M-38510 for coplanarity measurement requirements.
- 19. Must be a dimensional difference of .020 inch (0.51 mm) between L1 and L2.

FIGURE 1. Case outline Y (18-terminal, .305" x .505"), rectangular chip carrier package - Continued.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER		REVISION LEVEL	SHEET
DAYTON, OHIO 45444		D	15

## Device types 01, 02, and 03

Case E



# Device types 01, 02, and 03

Cases X and Y

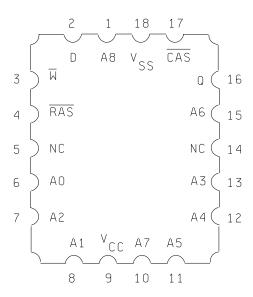


FIGURE 2. Terminal connections.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER		REVISION LEVEL	SHEET
DAYTON, OHIO 45444		D	16

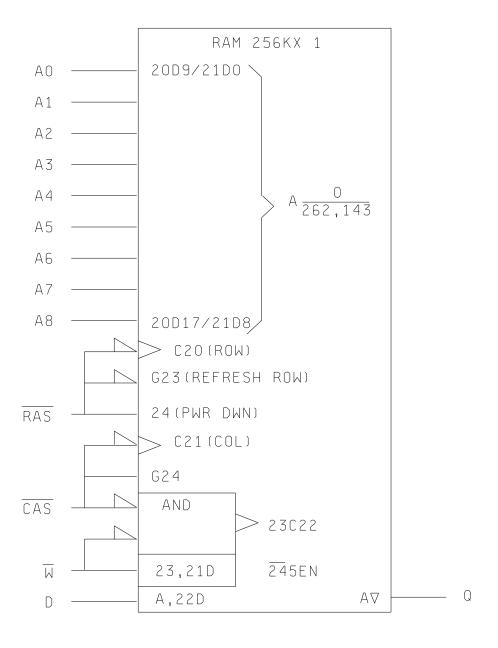
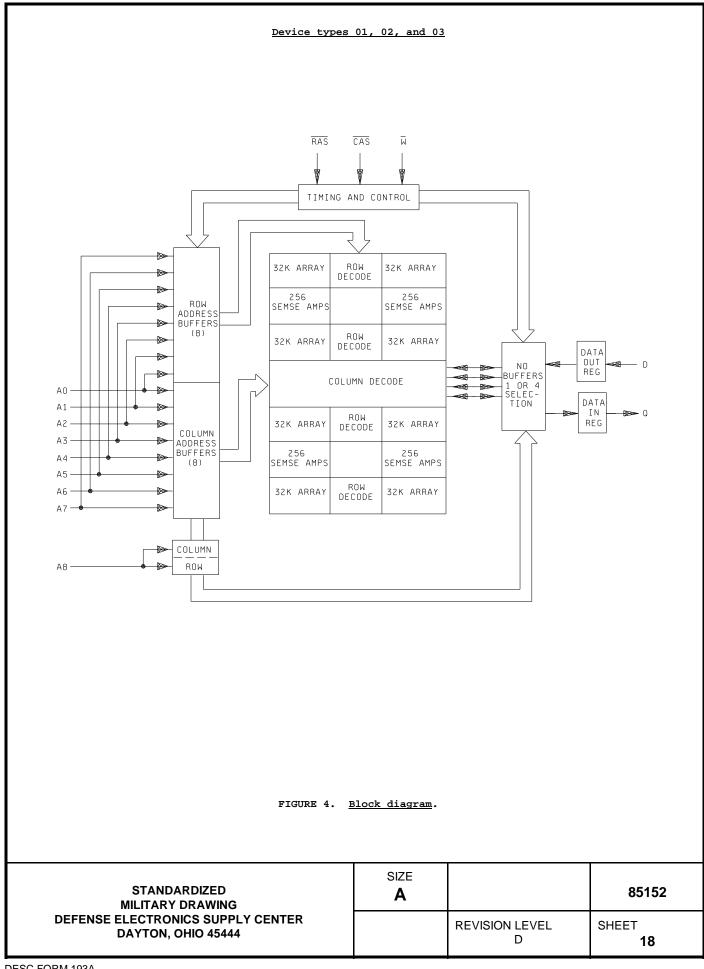


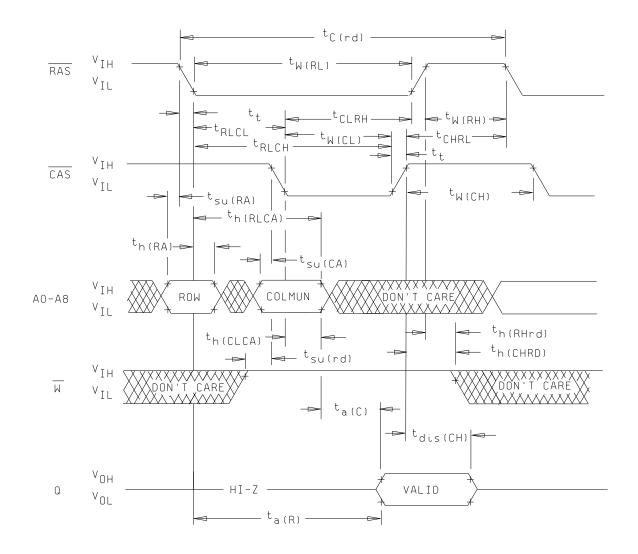
FIGURE 3. Logic diagram.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET <b>17</b>



## Read cycle timing

## Device types 01, 02, and 03



NOTE: Outputs are referenced to: Hi-Z to active state,  $V_{\rm OH}$  minimum or  $V_{\rm OL}$  maximum; active state to Hi-Z,  $V_{\rm OH}$  -.5 V or  $V_{\rm OL}$  +.5 V.

FIGURE 5. Switching waveforms.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER		REVISION LEVEL	SHEET
DAYTON, OHIO 45444		D	19

### Early cycle timing

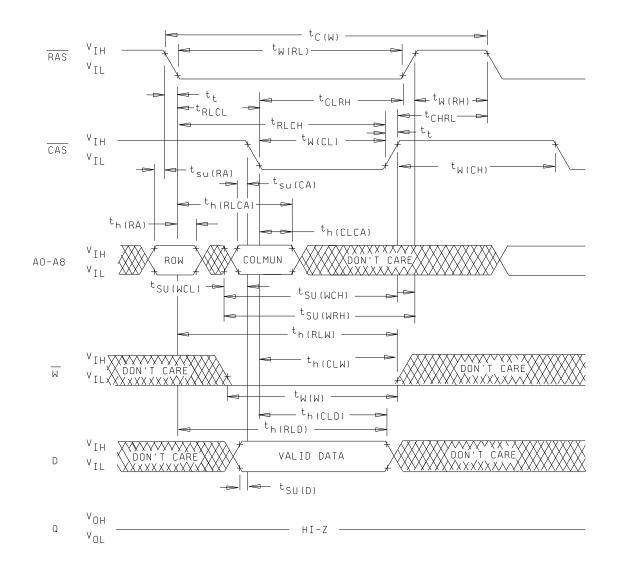
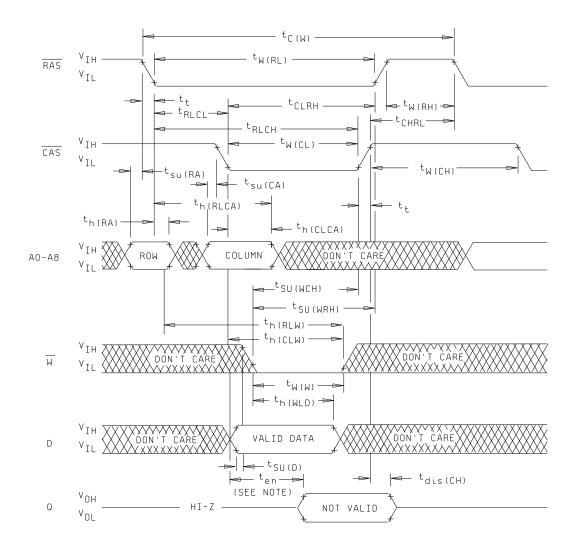


FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET <b>20</b>

## Write cycle timing

## Device types 01, 02, and 03



NOTE:  $\underline{\text{The}}$  enable time (t<sub>en</sub>) for a write cycle is equal in duration to the access time from CAS (t<sub>a(c)</sub>) in a read cycle; but the active levels at the output are invalid.

FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING	SIZE <b>A</b>		85152
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444		REVISION LEVEL D	SHEET <b>21</b>

# Read-write/read-modify-write cycle timing

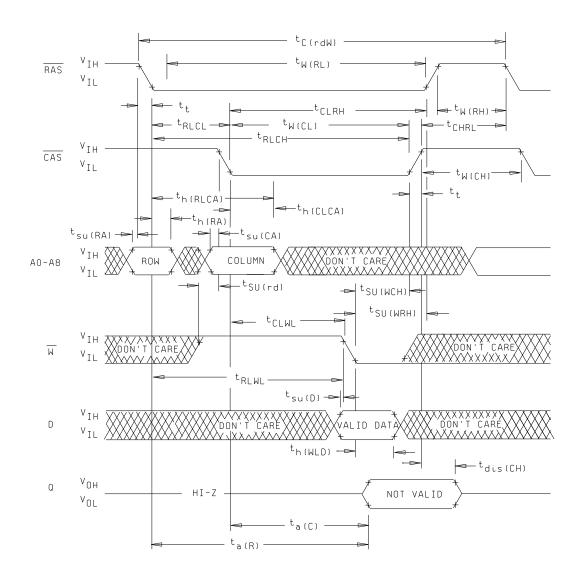


FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET <b>22</b>

Page-mode read cycle timing

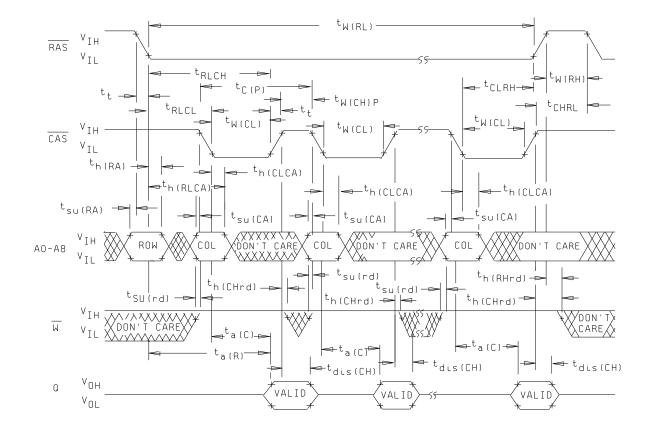


FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET 23

### Page-mode write cycle timing

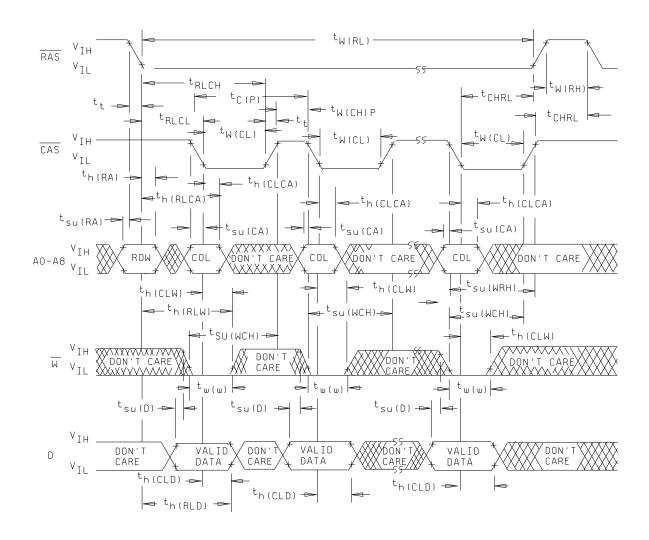


FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET <b>24</b>

## Page-mode read-modify-write cycle timing

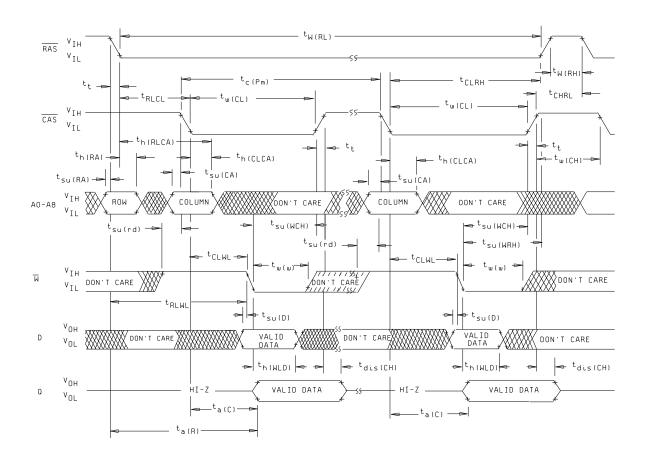


FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET <b>25</b>

RAS-only refresh cycle timing

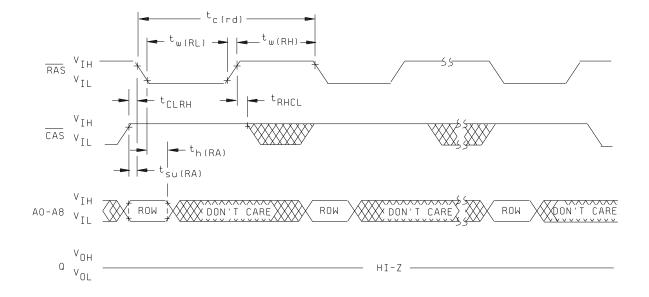


FIGURE 5. Switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET 26

## Hidden refresh cycle timing

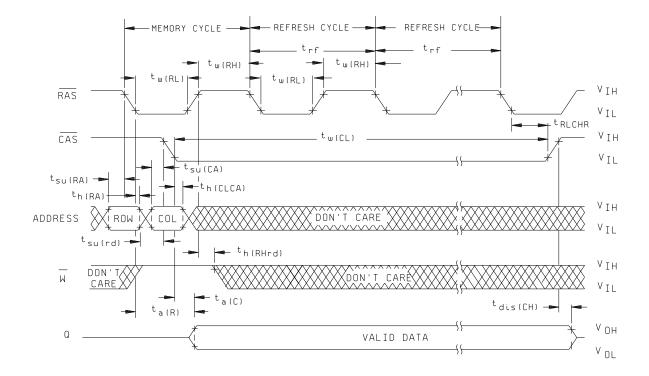


FIGURE 5. <u>Switching waveforms</u> - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET <b>27</b>

## Automatic $\overline{\text{CAS}}$ - before $\overline{\text{RAS}}$ refresh cycle timing

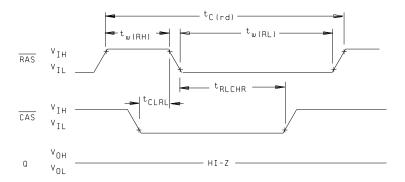


FIGURE 5. Switching waveforms - Continued.

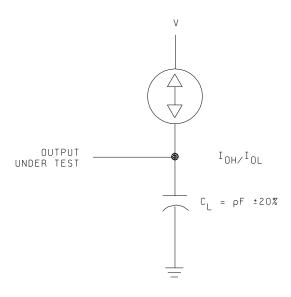


FIGURE 6. Load circuit.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE <b>A</b>		85152
		REVISION LEVEL D	SHEET <b>28</b>

- 4.3.2 Groups C and D inspections.
  - a. End-point electrical parameters shall be as specified in table II herein.
  - b. Steady-state life test conditions, method 1005 of MIL-STD-883:
    - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).
    - (2)  $T_A = +125^{\circ}C$ , minimum.
    - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 5. PACKAGING
- 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.
- 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.
- 6.2 Replaceability. Replaceability is determined as follows:
  - a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
  - b. When a QPL source is established, the device specified in this drawing will be replaced by the microcircuit identified as PIN M38510/2460XB\*X.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).
- 6.4 <u>Record of users</u>. Military and industrial users shall inform the Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6047.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.
- 6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE <b>A</b>		85152
	REVISION LEVEL D	SHEET <b>29</b>

### STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 92-07-27

Approved sources of supply for SMD 85152 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor <u>1</u> / similar PIN	Replacement military specification PIN
8515201EX	01295 6Y440 50088	SMJ4256-15JDS MT1259C-15 883C MKX45F56P-82	M38510/24604BEX
8515201XX	<u>2</u> / 6Y440	SMJ4256-15FVS MT1259EC-15 883	M38510/24604BXX
8515201YX	01295	SMJ4256-15FVS	
8515202EX	01295 6Y440 50088	SMJ4256-20JDS MT1259C-20 883C MKX45F56P-83	
8515202XX	2/ 6Y440	SMJ4256-20FVS MT1259EC-20 883	
8515202YX	01295	SMJ4256-20FVS	
8515203EX	01295 50088 6Y440	SMJ4256-12JDS MKX45F56P-81 MT1259C-12 883C	M38510/24603BEX
8515203XX	<u>2</u> / 6Y440	SMJ4256-12FVS MT1259EC-12 883C	M38510/24603BXX
8515203YX	01295	SMJ4256-12FVS	

- $\underline{1}/$  Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- $\underline{2}/\,\,$  No longer available from approved source of supply.

Vendor CAGE number	Vendor name <u>and address</u>
01295	Texas Instruments, Incorporated P.O. Box 6448 Midland, TX 79711
6Y440	Micron Technology, Incorporated 2805 East Columbia Road Boise, ID 83706
50088	SGS-Thomson Microelectronics 1310 Electronics Drive Carrollton, TX 75006

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